Practitioner's Docket No. AP9722

CHAPTER II

TRANSMITTAL LETTER TO THE UNITED STATES ELECTED OFFICE (EO/US)

(ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/EP00/08398	29/Aug/2000	22/Sept/1999
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED

System for Storing Data Words in a RAM Module
TITLE OF INVENTION

Wolfgang Fey, Adrian Traskov, Jan Truoel
APPLICANT(S)

Box PCT
Assistant Commissioner for Patents
Washington D.C. 20231
ATTENTION: EO/US

NOTE: To avoid abandonment of the application, the applicant shall furnish to the USPTO, not later than 20 months from the priority date: (1) a copy of the international application, unless it has been previously communicated by the International Bureau or unless it was originally filed in the USPTO; and (2) the basic national fee (see 37 C.F.R. § 1.492(a)). The 30-month time limit may not be extended. 37 C.F.R. § 1.495.

WARNING: *Where the items are those which can be submitted to complete the entry of the international application into the*

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national phase are subsequent to 30 months from the priority date the application is still considered to be in the international state and if mailing procedures are utilized to obtain a date the express mail procedure of 37 C.F.R. §1.10 must be used (since international application papers are not covered by an ordinary certificate of mailing - See 37 C.F.R. §1.8.

NOTE: *Documents and fees must be clearly identified as a submission to enter the national state under 35 USC 371 otherwise the submission will be considered as being made under 35 USC 111. 37 C.F.R. § 1.494(f).*

1. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. 371:

   a. [X] This express request to immediately begin national examination procedures (35 U.S.C. 371(f)).

   b. [X] The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees (37 C.F.R. § 1.492) as indicated below:

2.Fees

CLAIMS FEE	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
[ ]*	TOTAL CLAIMS	12 - 20 =		x $ 18.00 =	$
	INDEPENDENT CLAIMS	2 - 3 =		x $ 84.00 =	
	MULTIPLE DEPENDENT CLAIM(S) (if applicable) + $280.00				
BASIC FEE**	[ ] U.S. PTO WAS INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where an International preliminary examination fee as set forth in § 1.482 has been paid on the international application to the U.S. PTO: [ ] and the international preliminary examination report states that the criteria of novelty, inventive step (non-obviousness) and industrial activity, as defined in PCT Article 33(2) to (4) have been satisfied for all the claims presented in the application entering the national stage (37 CFR 1.492(a)(4)) ..... $100.00 [ ] and the above requirements are not met (37 CFR 1.492(a)(1)) ..... $710.00 [X] U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in § 1.445(a)(2) to the U.S. PTO: [ ] has been paid (37 CFR 1.492(a)(2)) ..... $740.00 [ ] has not been paid (37 CFR 1.492(a)(3)) ..... $1040.00 [X] where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 CFR 1.492(a)(5)) $890.00				
	Total of above Calculations				= 890.00
SMALL ENTITY	Reduction by ½ for filing by small entity, if applicable. Affidavit must be filed. (note 37 CFR 1.9, 1.27, 1.28)				-
	Subtotal				890.00
	Total National Fee				$ 890.00
	Fee for recording the enclosed assignment document $40.00 (37 CFR 1.21(h)). (See Item 13 below). See attached "ASSIGNMENT COVER SHEET".				
TOTAL	Total Fees enclosed				$ 890.00

*See attached Preliminary Amendment Reducing the Number of Claims.

i. [ ] A check in the amount of _____ to cover the above fees is enclosed.

ii. [X] Please charge Account No. 18-0013 in the amount of $ 890.00. A duplicate copy of this sheet is enclosed.

**WARNING: *"To avoid abandonment of the application the applicant shall furnish to the United States Patent and Trademark Office not later than the expiration of 30 months from the priority date: * * * (2) the basic national fee (see § 1.492(a)). The 30-month time limit may not be extended." 37 C.F.R. § 1.495(b).*

WARNING: *If the translation of the international application and/or the oath or declaration have not been submitted by the applicant within thirty (30) months from the priority date, such requirements may be met within a time period set by the Office. 37 C.F.R. § 1.495(b)(2). The payment of the surcharge set forth in § 1.492(e) is required as a condition for accepting the oath or declaration later than thirty (30) months after the priority date. The payment of the processing fee set forth in § 1.492(f) is required for acceptance of an English translation later than thirty (30) months after the priority date. Failure to comply with these requirements will result in abandonment of the application. The provisions of § 1.136 apply to the period which is set. Notice of Jan. 3, 1993, 1147 O.G. 29 to 40.*

3. [X] A copy of the International application as filed (35 U.S.C. 371(c)(2)):

NOTE: *Section 1.495 (b) was amended to require that the basic national fee and a copy of the international application must be filed with the Office by 30 months from the priority date to avoid abandonment "The International Bureau normally provides the copy of the international application to the Office in accordance with PCT Article 20. At the same time, the International Bureau notifies applicant of the communication to the Office. In accordance with PCT Rule 47.1, that notice shall be accepted by all designated offices as conclusive evidence that the communication has duly taken place. Thus, if the applicant desires to enter the national stage, the applicant normally need only check to be sure the notice from the International Bureau has been received and then pay the basic national fee by 30 months from the priority date." Notice of Jan. 7, 1993, 1147 O.G. 29 to 40, at 35-36. See item 14c below.*

a. [X] is transmitted herewith.

b. [ ] is not required, as the application was filed with the United States Receiving Office.

c. [ ] has been transmitted

i. [ ] by the International Bureau.
Date of mailing of the application (from form PCT/IB/308): _____.

ii. [ ] by applicant on _____.
Date

4. [X] A translation of the International application into the English language (35 U.S.C. 371(c)(2)):

a. [X] is transmitted herewith.

b. [ ] is not required as the application was filed in English.

c. [ ] was previously transmitted by applicant on _____.
Date

d. [ ] will follow.

5. [ ] Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. 371(c)(3)):

NOTE: The Notice of January 7, 1993 points out that 37 C.F.R. § 1.495(a) was amended to clarify the existing and continuing practice that PCT Article 19 amendments must be submitted by 30 months from the priority date and this deadline may not be extended. The Notice further advises that: "The failure to do so will not result in loss of the subject matter of the PCT Article 19 amendments. Applicant may submit that subject matter in a preliminary amendment filed under section 1.121. In many cases, filing an amendment under section 1.121 is preferable since grammatical or idiomatic errors may be corrected." 1147 O.G. 29-40, at 36.

a. [ ] are transmitted herewith.
b. [ ] have been transmitted
   i. [ ] by the International Bureau.
   Date of mailing of the amendment (from form PCT/IB/308): _____.
   ii. [ ] by applicant on _____.
   Date
c. [ ] have not been transmitted as
   i. [ ] applicant chose not to make amendments under PCT Article 19.
   Date of mailing of Search Report (from form PCT/ISA/210): _____.
   ii. [ ] the time limit for the submission of amendments has not yet expired. The amendments or a statement that amendments have not been made will be transmitted before the expiration of the time limit under PCT Rule 46.1.

6. [ ] A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. 371(c)(3)):
   a. [ ] is transmitted herewith.
   b. [ ] is not required as the amendments were made in the English language.
   c. [ ] has not been transmitted for reasons indicated at point 5(c) above.

7. [x] A copy of the international examination report (PCT/IPEA/409)
   [x] is transmitted herewith.
   [ ] is not required as the application was filed with the United States Receiving Office.

8. [ ] Annex(es) to the international preliminary examination report
   a. [ ] is/are transmitted herewith.
   b. [ ] is/are not required as the application was filed with the United States Receiving Office.

9. [ ] A translation of the annexes to the international preliminary examination report
   a. [ ] is transmitted herewith.
   b. [ ] is not required as the annexes are in the English language.

10. [X] An oath or declaration of the inventor (35 U.S.C. 371(c)(4)) complying with 35 U.S.C. 115
   a. [ ] was previously submitted by applicant on _____.
   Date
   b. [x] is submitted herewith, and such oath or declaration
      i. [x] is attached to the application.
      ii. [ ] identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. 1.70.

iii. [ ] will follow.

Other document(s) or information included:

11. [x] An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a):
    a. [x] is transmitted herewith.
    b. [ ] has been transmitted by the International Bureau.
       Date of mailing (from form PCT/IB/308): _____.
    c. [ ] is not required, as the application was searched by the United States International Searching Authority.
    d. [ ] will be transmitted promptly upon request.
    e. [ ] has been submitted by applicant on _____.
       Date

12. [X] An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98:
    a. [X] is transmitted herewith.
       Also transmitted herewith is/are:
       [X] Form PTO-1449 (PTO/SB/08A and 08B).
       [X] Copies of citations listed.
    b. [ ] will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. 371(c).
    c. [ ] was previously submitted by applicant on _____.
       Date

13. [x] An assignment document is transmitted herewith for recording.

A separate [x] "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or[ ] FORM PTO 1595 is also attached.

_____
_____
_____

14. [X] Additional documents:
    a. [ ] Copy of request (PCT/RO/101)
    b. [x] International Publication No. WO01/22225
       i. [ ] Specification, claims and drawing
       ii. [x] Front page only
    c. [X] Preliminary amendment (37 C.F.R. § 1.121)
    d. [ ] Other

_____
_____
_____

15. [X] The above checked items are being transmitted

a. [X] before 30 months from any claimed priority date.
b. [ ] after 30 months.

16. [ ] Certain requirements under 35 U.S.C. 371 were previously submitted by the applicant on ____________, namely:

____
____
____

AUTHORIZATION TO CHARGE ADDITIONAL FEES

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges if extra claims are authorized.*

NOTE: *"A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).*

NOTE: *"Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).*

[X] The Commissioner is hereby authorized to charge the following additional fees that may be required by this paper and during the entire pendency of this application to Account No. 18-0013.

[X] 37 C.F.R. 1.492(a)(1), (2), (3), and (4) (filing fees)

WARNING: *Because failure to pay the national fee within 30 months without extension (37 C.F.R. § 1.495(b)(2)) results in abandonment of the application, it would be best to always check the above box.*

[X] 37 C.F.R. 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: *Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possible when dealing with amendments after final action.*

[X] 37 C.F.R. 1.17 (application processing fees)
[X] 37 C.F.R. 1.17(a)(1)-(5)(extension fees pursuant to § 1.136(a).
[ ] 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

NOTE: *Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of*

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allowance. 37 C.F.R. § 1.311(b).

NOTE: *37 C.F.R. 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying . . . issue fee." From the wording of 37 C.F.R. § 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.*

[X] 37 C.F.R. § 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).

SIGNATURE OF PRACTITIONER

Reg. No.: 33,373

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APPLICATION DATA SHEET (AP9722)

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APPLICATION INFORMATION

Title Line One:	Sensor for Storing Data Words in a RAM Module
Total Drawings Sheets:	3
Formal Drawings?:	yes
Application Type:	Utility
Docket Number::	AP9722
Secrecy Order in Parent Appl.?::	No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 010291

CONTINUITY INFORMATION

This application was filed on 29/Aug/2000 as PCT International Application No. PCT/EP00/08398 and claims priority under 35 USC §119(a)-(d) or §365(b) to German Application No. 19945494.9 filed 22/Sept/1999 and German Application No. 10018722.6 filed 15/April/2000.

AP9722

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Fey et al.

Int'l Application No.: PCT/EP00/08398

Int'l Filing Date: 29/August/2000

Serial No.: Group Art Unit:

Filed: Herewith Examiner:

For: System for Storing Data Words in a RAM Module

Attorney Docket No.: AP9722 Paper No.

Box PCT
Commissioner of Patents
Washington, D.C. 20231
Attn: EO/US

CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

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Date: 3/22/02

☐ transmitted by facsimile to the Patent and Trademark Office. to Examiner _____ at _____

Signature Joyce Krumpe

Joyce Krumpe

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the application as follows prior to examination on the merits.

IN THE TITLE

Please amend the title everywhere except in the Declaration to read as follows:

-- System for Storing Data Words in a RAM Module --

IN THE CLAIMS

Please cancel claims 1-12 and add the following new claims.

13. (New) Method of storing data words in a RAM module, comprising the steps of:

producing a check bit word from at least one data word when writing the at least one data word into the RAM module,

storing the check bit word,

reading out the check bit word when reading out the at least one data word from the RAM module,

regenerating the check bit word from the at least one read-out data word,

comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

14. (New) Method as claimed in claim 13, wherein the check bit word is generated by determining parity bits.

15. (New) Method as claimed in claim 14, wherein a 2 bit parity word is generated from each data word, and one parity bit is respectively determined from each half of the data word.

16. (New) Method as claimed in claim 13, wherein the check bit word is generated from a plurality of data words, and parity bits of the check bit word are respectively determined from equal digits of all data words.

17. (New) Method as claimed in claim 13, wherein the check bit words are generated by calculating CRC words.

18. (New) Method as claimed in claim 17, wherein a memory word is formed by summing a plurality of data words, and wherein an associated CRC word is calculated therefrom.

19. (New) Circuit configuration for storing data words in a RAM module, comprising:

a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word,

a plurality of registers for the allocated storage of check bit words for the data words, and

a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond.

20. (New) Circuit configuration as claimed in claim 19, wherein the number of registers in said plurality of registers is determined by including one 2-bit parity register for each data word.

21. (New) Circuit configuration as claimed in claim 19, wherein the number of registers in said plurality of registers is determined by including one CRC register for each four data words.

22. (New) Circuit configuration as claimed in claim 21, further including a multiplexer for storing four data words as one memory word, and a CRC arithmetic unit for calculating the CRC word from a memory word and for storing the CRC word in an associated CRC register.

23. (New) Circuit configuration as claimed in claim 22, wherein the data words are 32 bits long and the CRC words are 9 bits long.

24. (New) Circuit configuration as claimed in claim 19, further including a global check bit word register for storing a global check bit word, the bits of which are respectively determined from equal digits of all data words, and an associated register for storing a check bit word which is determined from the contents of the global register.

REMARKS

Prior to a formal examination of the above-identified application, acceptance of the new claims and the enclosed substitute specification (under 37 CFR 1.125) is respectfully requested. It is believed that the substitute specification and new claims will facilitate processing of the application in accordance with M.P.E.P. 608.01(q). The substitute specification and new claims are in compliance with 37 CFR 1.52 (a and b) and, while making no substantive changes, are submitted to conform this case to the formal requirements and long-established formal standards of U.S. Patent Office practice, and to provide improved idiom and better grammatical form.

The enclosed substitute specification is presented herein in both marked-up and clean versions.

STATEMENT

The undersigned, an attorney registered to practice before the office, hereby states that the enclosed substitute specification includes the same changes as are indicated in the mark-up copy of the original specification. The substitute specification contains no new subject matter.

Respectfully submitted,

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SUBSTITUTE SPECIFICATION: CLEAN COPY

AP9722

System for Storing Data Words in a RAM Module

Technical Field

[01] The present invention generally relates to memory storage systems and more particularly relates to a method and a circuit configuration for storing data words in a RAM module.

Background of The Invention

[02] RAM (Random Access Memory) modules are generally known in the art and common in use. They are employed for repeatedly storing and reading out data for a great number of applications. Special attention must be paid to the integrity of data stored in the RAM module when designing the memory architecture. In a prior art scheme, data integrity is ensured by a fully redundant design of the module in a relatively reliable fashion. A major shortcoming in this respect is, however, that the financial cost is relatively high.

[03] In view of the above, an object of the present invention is to provide a method and a circuit configuration for storing data words in a RAM module whose demand in junction is considerably lower, without suffering from limitations with respect to data integrity.

[04] This object is achieved by a method according to the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the

check bit word when reading out the at least one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

[05] Further, the object is achieved by a circuit configuration according to claim 7 which is characterized by: a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word, a number of registers for the associated storage of check bit words for the data words, and a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond.

[06] A special advantage of this solution involves that in the event of basically equal data integrity as in the above-mentioned fully redundant design, the necessary silicon junction and, hence, the circuit design effort and costs is considerably lower.

Brief Description of The Drawings

[07] Figure 1 is a schematic view of a first memory scheme.

[08] Figure 2 is a schematic view of the course of a writing operation.

[09] Figure 3 is a schematic view of the course of a reading operation.

[10] Figure 4 shows the generation of a word-oriented parity.

[11] Figure 5 is a schematic view of a second memory scheme.

[12] Figure 6 shows the generation of a column-oriented parity.

Detailed Description of The Preferred Embodiments

[13] According to Figure 1, a RAM module generally comprises a word-oriented array 10 made up of a number of 32 bit data word registers 10a, ..10, ...10x which are illustrated as being arranged one below the other in rows. A 2 bit parity word register 11a,...11i,...11x is associated with each data word register so that a 2 bit parity array 11 is the result. There is further provision of a 2 bit parity word register 12 allocated to which, in turn, is a 2 bit parity word register 13.

[14] For the purpose of data exchange, this arrangement is connected in a known fashion to a bus interface 14 by means of which a connection to a CPU bus can be established. The bus interface 14 further comprises circuit units for generating and comparing the parity words in writing and reading operations which are illustrated in Figures 2 and 3.

[15] For writing into the RAM module, the respective data words are sent by a 32 bit data bus 20 to a first circuit unit 21 used to generate a 2 bit parity word with respect to each data word according to Figure 2. Subsequently, the data word is written into one of the data word registers 10i in

the RAM module, and the 2 bit parity word is written into the associated 2 bit parity word register 11i.

[16] To read data words out of the RAM module, the addressed data word is initially sent to the first circuit unit 21. The associated 2 bit parity word is simultaneously transmitted into a second circuit unit 22. In the first circuit unit 21, in turn, a 2 bit parity word is generated from the read-out data word and sent to the second circuit unit 22, where it is compared with the 2 bit parity word directly read out of the RAM module. If these two words do not correspond, an error signal F is produced or a corresponding error flag is set. If the 2 bit parity words correspond, the read-out data word is transmitted to the data bus 20.

[17] According to Figure 4, each 32 bit data word is composed of a first and a second 16 bit halfword HW, and a bit B of the 2 bit parity word is generated from each halfword.

[18] Individual bit errors may be detected at once 'online' when reading out of the RAM module due to the automatic generation and the automatic comparison of these word-oriented parities.

[19] To reach a still greater safety of error prevention, the 2 bit parity generation may also be replaced by a CRC (Cyclic Redundancy Check) check with a CRC word calculated for each data word according to a polynomial. To achieve an expedient ratio between the length of a data word and the length of a CRC word, the memory scheme is chosen so that the length of the stored data words (memory words) is a multiple of the length of the data words on the data bus. In

the event of a data word length of 32 bit, the memory word preferably has a length of 128 bit and the CRC word for an optimal error prevention safety has a length of 9 bit.

[20] Figure 5 shows a corresponding arrangement which is connected to a 32 bit data bus (not shown) by way of the bus interface 14.

[21] The RAM module comprises an array 60 made up of a number of 128 bit memory word registers 60a,...60x which are shown as being arranged one below the other in rows. Associated with each memory word register is a CRC register 61a,...61x with e.g. 9 bits in each case so that a CRC array 61 is achieved.

[22] Interconnected between the array 60 and the bus interface 14 is a unit 70 which includes a multiplexer 71 for 32 bit data words each and a 128 bit CRC arithmetic register 72 for receiving four 32 bit data words. Further, unit 70 comprises a CRC arithmetic unit 73, by means of which a 9 bit CRC word is calculated from the contents of the 128 bit CRC arithmetic register 72 by known calculation methods and intermediately stored in a 9 bit CRC register 74 which, in turn, is connected to the bus interface 14.

[23] The writing and reading operations basically take place in the same manner as shown in Figures 2 and 3.

[24] In the operation of writing into the RAM module, four 32 bit data words which are input by way of the bus interface 14 are cyclically stored consecutively in the 128 bit CRC arithmetic register 72 by means of the multiplexer 71 so that a 128 bit memory word is achieved. From this the 9 bit

CRC word is calculated with the CRC arithmetic unit 73 and registered in the 9 bit CRC register 74. Subsequently, the contents of the 128 bit CRC arithmetic register 72 is stored in one of the 128 bit memory word registers 60i of the RAM array, and the contents of the 9 bit CRC register 74 is stored in the associated 9 bit CRC word register 61i.

[25] When writing a new 32 bit data word (or shorter word units) into the RAM module, it is necessary to recalculate the CRC word of the respective 128 bit memory word register 60i. This means that before writing the new data word, it is first necessary to fully read out the contents of the respective 128 bit memory word register 60i and to store it in the CRC arithmetic register 72. Subsequently, the 9 bit CRC word is recalculated with the CRC arithmetic unit 73 on the basis of the new data word and stored in the CRC register 74. The contents of both registers 72, 74 are then transferred into the corresponding registers 60i, 61i.

[26] If it is desired to perform an error check before writing a new 32 bit data word, which check may be triggered in defined intervals by e.g. a software, initially, the contents of the respective 128 bit memory word register 609 and the contents of the associated CRC register 61i is read out, as mentioned above. Thereafter, the 9 bit CRC word is regenerated therefrom by CRC arithmetic unit 73 and compared with the read-out CRC word. If these two CRC words do not correspond, an error signal F (or a corresponding error flag) is produced. If the CRC words correspond, a new 9 bit CRC word is calculated from the 128 bit memory word which contains the new 32 bit data word, as has been explained hereinabove, and both are read in the corresponding 128 bit

memory word register 60i or the associated 9 bit CRC register 61i of the RAM module, respectively.

[27] The error check can be performed even if it is desired to read out a data word from the RAM module on the data bus 20. For this purpose, the contents of the memory word register 60i that contains the respective data word is transferred into the CRC arithmetic register 72, and the CRC word is recalculated therefrom. This CRC word is compared to the CRC word memorized in the associated CRC word register 61i. If the two words do not correspond, an error message F is generated or a corresponding error flag set. If both CRC words correspond, the read-out 32 bit data word is transferred to the data bus 20. Thereafter, the contents of the CRC arithmetic register 72 is returned into the corresponding 128 bit memory word register 60i.

[28] Figure 6 shows several memory word registers 10a, 10b,..10x, for 32 bit data words and a 32 bit parity word register 12, wherein a bit with the value 0 or 1 is illustrated for each digit as an example.

[29] In contrast to the word-oriented check bit generation shown in Figures 4 and 5, a column-oriented parity is generated according to Figure 6, wherein for respectively equal digits of all data words a parity bit is determined which is written into an associated digit in the 32 bit parity word register 32. A 32 bit parity word is thus achieved. Further, a 2 bit parity word can be generated and stored in the 2 bit parity word register 13 (see Figure 1) with respect to the above 32 bit parity word in the same manner as was described for the word-oriented parity by way of Figure 4. Corresponding to the fashion described

hereinabove, a column-oriented parity check can be performed in the embodiment of Figure 5 with 128 bit long data words.

[30] When writing a new data word in one of the word registers 10i of the RAM module, first the contents of the data word of the memory digit being described in the RAM module, i.e., a 32 bit data word register 10i in the present example, and the 32 bit parity word register 12 is read out. Thereafter, the value of the column-oriented 32 bit parity word is determined and described again.

[31] Subsequently, the new data word is re-written in the corresponding data word registers 10i, and the contents of the 32 bit parity word register 12 is re-determined. Following this operation, again a 2 bit parity can be generated with respect to the 32 bit parity word and stored in the 2 bit parity word register 13 (see Figure 1).

[32] It is preferred that an error check is not performed during a normal reading operation. An additional error check may be carried out in that in the manner described above, e.g. at the point of time during a reading operation, the contents of all data word registers 10i is read out, the column-oriented 32 bit parity word is regenerated and compared with the parity word stored in the parity word register 12. If the parity words do not correspond, an error message F is produced or a corresponding error flag is set. If the parity words correspond, the read-out data word is transferred to the data bus 20. The column-oriented error check in the entire RAM described in the embodiment hereinabove is expediently not performed with each writing or reading operation but at defined intervals, and it is possible that the said intervals are predetermined by the

software used. The decision whether this error check takes place or not is preferably made by the implemented software.

[33] The 2 bit parity word of the 32 bit parity word can be used for error checks in the same way as it was described by way of Figures 2 to 4 for the 2 bit parity words of the data words.

[34] Instead of the column-oriented parity, a column-oriented CRC (Cyclic Redundancy Check) sum may be produced and used for error checks. Before writing and/or reading a word, first the contents of all data word registers 10i and check bit register 12 are read out, and the CRC word is determined again also in this case. If this CRC word does not correspond with the memorized CRC word, an error message F is produced or a corresponding error flag is set. If both CRC words correspond, the writing or reading operation is concluded in the manner described in the above with respect to the column-oriented parity word generation.

[35] The column-oriented parity and a cyclically occurring parity check or the CRC check sum and a cyclic CRC calculation permit detecting errors in the address decoder as well as double bit errors and further errors. The checks or calculations, respectively, are preferably performed by a corresponding software.

System for Storing Data Words in a RAM Module

Abstract of The Disclosure

The present invention describes a method of storing data words in a RAM module which is especially suited for applications that are critical in terms of safety and includes the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the check bit word when reading out the at least one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond. This invention further relates to a corresponding circuit configuration.

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[PC 9722]

[Method and Circuit Configuration] System for Storing Data Words in a RAM Module

Technical Field

The present invention generally relates to memory storage systems and more particularly relates to a method and a circuit configuration for storing data words in a RAM module[, especially suited for applications that are critical in terms of safety].

Background of The Invention

RAM (Random Access Memory) modules are generally known in the art and common in use. They are employed for repeatedly storing and reading out data for a great number of applications. Special attention must be paid to the integrity of data [memorized] stored in the RAM module when designing the memory architecture. In a prior art scheme, data integrity is ensured by a fully redundant design of the module in a relatively reliable fashion. A major shortcoming in this respect is, however, that the [expenditure in circuit structure and the demand in silicon junction] financial cost is relatively high.

In view of the above, an object of the present invention is to provide a method and a circuit configuration for storing data words in a RAM module whose demand in junction is considerably

lower, without suffering from limitations with respect to data integrity.

This object is achieved by a method according to [claim 1 which is characterized by] the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the check bit word when reading out the at least one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

Further, the object is achieved by a circuit configuration according to claim 7 which is characterized by: a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word, a number of registers for the associated storage of check bit words for the data words, and a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond.

A special advantage of this solution involves that in the event of basically equal data integrity as in the above-mentioned fully redundant design, the necessary silicon junction and, hence, the circuit design effort and costs is considerably lower.

[The subclaims are directed to favorable improvements of the present invention.

Further details, features, and advantages of the present invention can be taken from the following description of a preferred embodiment by making reference to the accompanying drawings. In the drawings,]

Brief Description of The Drawings

Figure 1 is a schematic view of a first memory scheme.

Figure 2 is a schematic view of the course of a writing operation.

Figure 3 is a schematic view of the course of a reading operation.

Figure 4 shows the generation of a word-oriented parity.

Figure 5 is a schematic view of a second memory scheme.

Figure 6 shows the generation of a column-oriented parity.

Detailed Description of The Preferred Embodiments

According to Figure 1, a RAM module generally comprises a word-oriented array 10 made up of a number of 32 bit data word registers 10a, ..10, ...10x which are illustrated as being arranged one below the other in rows. A 2 bit parity word register 11a,...11i,...11x is associated with each data word register so that a 2 bit parity array 11 is the result. There is further provision of a 2 bit parity word register 12 allocated to which, in turn, is a 2 bit parity word register 13.

For the purpose of data exchange, this arrangement is connected in a known fashion to a bus interface 14 by means of which a connection to a CPU bus can be established. The bus interface 14 further comprises circuit units for generating and comparing the parity words in writing and reading operations which are illustrated in Figures 2 and 3.

For writing into the RAM module, the respective data words are sent by a 32 bit data bus 20 to a first circuit unit 21 used to generate a 2 bit parity word with respect to each data word according to Figure 2. Subsequently, the data word is written into one of the data word registers 10i in the RAM module, and the 2 bit parity word is written into the associated 2 bit parity word register 11i.

To read data words out of the RAM module, the addressed data word is initially sent to the first circuit unit 21. The associated 2 bit parity word is simultaneously transmitted into a second circuit unit 22. In the first circuit unit 21, in turn, a 2 bit parity word is generated from the read-out data word and sent to the second circuit unit 22, where it is compared with the 2 bit parity word directly read out of the RAM module. If these two words do not correspond, an error signal F is produced or a corresponding error flag is set. If the 2 bit parity words correspond, the read-out data word is transmitted to the data bus 20.

According to Figure 4, each 32 bit data word is composed of a first and a second 16 bit halfword HW, and a bit B of the 2 bit parity word is generated from each halfword.

Individual bit errors may be detected at once 'online' when reading out of the RAM module due to the automatic generation and the automatic comparison of these word-oriented parities.

To reach a still greater safety of error prevention, the 2 bit parity generation may also be replaced by a CRC (Cyclic Redundancy Check) check with a CRC word calculated for each data word according to a polynomial. To achieve an expedient ratio between the length of a data word and the length of a CRC word, the memory scheme is chosen so that the length of the stored data words (memory words) is a multiple of the length of the data words on the data bus. In the event of a data word length of 32 bit, the memory word preferably has a length of 128 bit and the CRC word for an optimal error prevention [saftey] safety has a length of 9 bit.

Figure 5 shows a corresponding arrangement which is connected to a 32 bit data bus (not shown) by way of the bus interface 14.

The RAM module comprises an array 60 made up of a number of 128 bit memory word registers 60a,...60x which are shown as being arranged one below the other in rows. Associated with each memory word register is a CRC register 61a,...61x with e.g. 9 bits in each case so that a CRC array 61 is achieved.

Interconnected between the array 60 and the bus interface 14 is a unit 70 which includes a multiplexer 71 for 32 bit data words each and a 128 bit CRC arithmetic register 72 for receiving four 32 bit data words. Further, unit 70 comprises a CRC arithmetic unit 73, by means of which a 9 bit CRC word is calculated from the contents of the 128 bit CRC arithmetic register 72 by known calculation methods and intermediately

stored in a 9 bit CRC register 74 which, in turn, is connected to the bus interface 14.

The writing and reading operations basically take place in the same manner as shown in Figures 2 and 3.

In the operation of writing into the RAM module, four 32 bit data words which are input by way of the bus interface 14 are cyclically stored consecutively in the 128 bit CRC arithmetic register 72 by means of the multiplexer 71 so that a 128 bit memory word is achieved. From this the 9 bit CRC word is calculated with the CRC arithmetic unit 73 and registered in the 9 bit CRC register 74. Subsequently, the contents of the 128 bit CRC arithmetic register 72 is stored in one of the 128 bit memory word registers 60i of the RAM array, and the contents of the 9 bit CRC register 74 is stored in the associated 9 bit CRC word register 61i.

When writing a new 32 bit data word (or shorter word units) into the RAM module, it is necessary to recalculate the CRC word of the respective 128 bit memory word register 60i. This means that before writing the new data word, it is first necessary to fully read out the contents of the respective 128 bit memory word register 60i and to store it in the CRC arithmetic register 72. Subsequently, the 9 bit CRC word is recalculated with the CRC arithmetic unit 73 on the basis of the new data word and stored in the CRC register 74. The contents of both registers 72, 74 are then transferred into the corresponding registers 60i, 61i.

If it is desired to perform an error check before writing a new 32 bit data word, which check may be triggered in defined intervals by e.g. a software, initially, the contents of the

respective 128 bit memory word register 609 and the contents of the associated CRC register 61i is read out, as mentioned above. Thereafter, the 9 bit CRC word is regenerated therefrom by CRC arithmetic unit 73 and compared with the read-out CRC word. If these two CRC words do not correspond, an error signal F (or a corresponding error flag) is produced. If the CRC words correspond, a new 9 bit CRC word is calculated from the 128 bit memory word which contains the new 32 bit data word, as has been explained hereinabove, and both are read in the corresponding 128 bit memory word register 60i or the associated 9 bit CRC register 61i of the RAM module, respectively.

The error check can be performed even if it is desired to read out a data word from the RAM module on the data bus 20. For this purpose, the contents of the memory word register 60i that contains the respective data word is transferred into the CRC arithmetic register 72, and the CRC word is recalculated therefrom. This CRC word is compared to the CRC word memorized in the associated CRC word register 61i. If the two words do not correspond, an error message F is generated or a corresponding error flag set. If both CRC words correspond, the read-out 32 bit data word is transferred to the data bus 20. Thereafter, the contents of the CRC arithmetic register 72 is returned into the corresponding 128 bit memory word register 60i.

Figure 6 shows several memory word registers 10a, 10b,..10x, for 32 bit data words and a 32 bit parity word register 12, wherein a bit with the value 0 or 1 is illustrated for each digit as an example.

In contrast to the word-oriented check bit generation shown in Figures 4 and 5, a column-oriented parity is generated according to Figure 6, wherein for respectively equal digits of all data words a parity bit is determined which is written into an associated digit in the 32 bit parity word register 32. A 32 bit parity word is thus achieved. Further, a 2 bit parity word can be generated and stored in the 2 bit parity word [regiser] register 13 (see Figure 1) with respect to the above 32 bit parity word in the same manner as was described for the word-oriented parity by way of Figure 4. Corresponding to the fashion described hereinabove, a column-oriented parity check can be performed in the embodiment of Figure 5 with 128 bit long data words.

When writing a new data word in one of the word registers 10i of the RAM module, first the contents of the data word of the memory digit being described in the RAM module, i.e., a 32 bit data word register 10i in the present example, and the 32 bit parity word register 12 is read out. Thereafter, the value of the column-oriented 32 bit parity word is determined and described again.

Subsequently, the new data word is re-written in the corresponding data word registers 10i, and the contents of the 32 bit parity word register 12 is re-determined. Following this operation, again a 2 bit parity can be generated with respect to the 32 bit parity word and stored in the 2 bit parity word register 13 (see Figure 1).

It is preferred that an error check is not performed during a normal reading operation. An additional error check may be carried out in that in the manner described above, e.g. at the point of time during a reading operation, the contents of all

data word registers 10i is read out, the column-oriented 32 bit parity word is regenerated and compared with the parity word stored in the parity word register 12. If the parity words do not correspond, an error message F is produced or a corresponding error flag is set. If the parity words correspond, the read-out data word is transferred to the data bus 20. The column-oriented error check in the entire RAM described in the embodiment hereinabove is expediently not performed with each writing or reading operation but at defined intervals, and it is possible that the said intervals are [prededetermined] predetermined by the software used. The decision whether this error check takes place or not is preferably made by the implemented software.

The 2 bit parity word of the 32 bit parity word can be used for error checks in the same way as it was described by way of Figures 2 to 4 for the 2 bit parity words of the data words.

Instead of the column-oriented parity, a column-oriented CRC (Cyclic Redundancy Check) sum may be produced and used for error checks. Before writing and/or reading a word, first the contents of all data word registers 10i and check bit register 12 are read out, and the CRC word is determined again also in this case. If this CRC word does not correspond with the memorized CRC word, an error message F is produced or a corresponding error flag is set. If both CRC words correspond, the writing or reading operation is concluded in the manner described in the above with respect to the column-oriented parity word generation.

The column-oriented parity and a cyclically occurring parity check or the CRC check sum and a cyclic CRC calculation permit

detecting errors in the address decoder as well as double bit errors and further errors. The checks or calculations, respectively, are preferably performed by a corresponding software.

[Abstract:]

[Method and Circuit Configuration] <u>**System**</u> **for Storing Data Words in a RAM Module**

<u>Abstract of The Disclosure</u>

The present invention describes a method of storing data words in a RAM module which is especially suited for applications that are critical in terms of safety and includes the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the check bit word when reading out the at least one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond. This invention further relates to a corresponding circuit configuration.

[(Figure 3)]

3/parts

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Method and Circuit Configuration for Storing Data Words in a RAM Module

The present invention relates to a method and a circuit configuration for storing data words in a RAM module, especially suited for applications that are critical in terms of safety.

RAM (Random Access Memory) modules are generally known in the art and common in use. They are employed for repeatedly storing and reading out data for a great number of applications. Special attention must be paid to the integrity of data memorized in the RAM module when designing the memory architecture. In a prior art scheme, data integrity is ensured by a fully redundant design of the module in a relatively reliable fashion. A major shortcoming in this respect is, however, that the expenditure in circuit structure and the demand in silicon junction is relatively high.

In view of the above, an object of the present invention is to provide a method and a circuit configuration for storing data words in a RAM module whose demand in junction is considerably lower, without suffering from limitations with respect to data integrity.

This object is achieved by a method according to claim 1 which is characterized by the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the check bit word when reading out the at least

one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

Further, the object is achieved by a circuit configuration according to claim 7 which is characterized by: a first circuit unit for generating a check bit word from at least one data word when writing and reading the at least one data word, a number of registers for the associated storage of check bit words for the data words, and a second circuit unit by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit, and for generating an error message if the check bit words do not correspond.

A special advantage of this solution involves that in the event of basically equal data integrity as in the above-mentioned fully redundant design, the necessary silicon junction and, hence, the circuit design effort and costs is considerably lower.

The subclaims are directed to favorable improvements of the present invention.

Further details, features, and advantages of the present invention can be taken from the following description of a preferred embodiment by making reference to the accompanying drawings. In the drawings,

Figure 1 is a schematic view of a first memory scheme.

Figure 2 is a schematic view of the course of a writing operation.

Figure 3 is a schematic view of the course of a reading operation.

Figure 4 shows the generation of a word-oriented parity.

Figure 5 is a schematic view of a second memory scheme.

Figure 6 shows the generation of a column-oriented parity.

According to Figure 1, a RAM module generally comprises a word-oriented array 10 made up of a number of 32 bit data word registers 10a, ..10, ...10x which are illustrated as being arranged one below the other in rows. A 2 bit parity word register 11a,...11i,...11x is associated with each data word register so that a 2 bit parity array 11 is the result. There is further provision of a 2 bit parity word register 12 allocated to which, in turn, is a 2 bit parity word register 13.

For the purpose of data exchange, this arrangement is connected in a known fashion to a bus interface 14 by means of which a connection to a CPU bus can be established. The bus interface 14 further comprises circuit units for generating and comparing the parity words in writing and reading operations which are illustrated in Figures 2 and 3.

For writing into the RAM module, the respective data words are sent by a 32 bit data bus 20 to a first circuit unit 21 used to generate a 2 bit parity word with respect to each data word according to Figure 2. Subsequently, the data word is written into one of the data word registers 10i in the RAM module, and the 2 bit parity word is written into the associated 2 bit parity word register 11i.

To read data words out of the RAM module, the addressed data word is initially sent to the first circuit unit 21. The associated 2 bit parity word is simultaneously transmitted into a second circuit unit 22. In the first circuit unit 21, in turn, a 2 bit parity word is generated from the read-out data word and sent to the second circuit unit 22, where it is compared with the 2 bit parity word directly read out of the RAM module. If these two words do not correspond, an error signal F is produced or a corresponding error flag is set. If the 2 bit parity words correspond, the read-out data word is transmitted to the data bus 20.

According to Figure 4, each 32 bit data word is composed of a first and a second 16 bit halfword HW, and a bit B of the 2 bit parity word is generated from each halfword.

Individual bit errors may be detected at once 'online' when reading out of the RAM module due to the automatic generation and the automatic comparison of these word-oriented parities.

To reach a still greater safety of error prevention, the 2 bit parity generation may also be replaced by a CRC (Cyclic Redundancy Check) check with a CRC word calculated for each data word according to a polynomial. To achieve an expedient ratio between the length of a data word and the length of a CRC word, the memory scheme is chosen so that the length of the stored data words (memory words) is a multiple of the length of the data words on the data bus. In the event of a data word length of 32 bit, the memory word preferably has a length of 128 bit and the CRC word for an optimal error prevention saftey has a length of 9 bit.

Figure 5 shows a corresponding arrangement which is connected to a 32 bit data bus (not shown) by way of the bus interface 14.

The RAM module comprises an array 60 made up of a number of 128 bit memory word registers 60a,...60x which are shown as being arranged one below the other in rows. Associated with each memory word register is a CRC register 61a,...61x with e.g. 9 bits in each case so that a CRC array 61 is achieved.

Interconnected between the array 60 and the bus interface 14 is a unit 70 which includes a multiplexer 71 for 32 bit data words each and a 128 bit CRC arithmetic register 72 for receiving four 32 bit data words. Further, unit 70 comprises a CRC arithmetic unit 73, by means of which a 9 bit CRC word is calculated from the contents of the 128 bit CRC arithmetic register 72 by known calculation methods and intermediately stored in a 9 bit CRC register 74 which, in turn, is connected to the bus interface 14.

The writing and reading operations basically take place in the same manner as shown in Figures 2 and 3.

In the operation of writing into the RAM module, four 32 bit data words which are input by way of the bus interface 14 are cyclically stored consecutively in the 128 bit CRC arithmetic register 72 by means of the multiplexer 71 so that a 128 bit memory word is achieved. From this the 9 bit CRC word is calculated with the CRC arithmetic unit 73 and registered in the 9 bit CRC register 74. Subsequently, the contents of the 128 bit CRC arithmetic register 72 is stored in one of the 128 bit memory word registers 60i of the RAM array, and the contents of the 9 bit CRC register 74 is stored in the associated 9 bit CRC word register 61i.

When writing a new 32 bit data word (or shorter word units) into the RAM module, it is necessary to recalculate the CRC word of the respective 128 bit memory word register 60i. This

means that before writing the new data word, it is first necessary to fully read out the contents of the respective 128 bit memory word register 60i and to store it in the CRC arithmetic register 72. Subsequently, the 9 bit CRC word is recalculated with the CRC arithmetic unit 73 on the basis of the new data word and stored in the CRC register 74. The contents of both registers 72, 74 are then transferred into the corresponding registers 60i, 61i.

If it is desired to perform an error check before writing a new 32 bit data word, which check may be triggered in defined intervals by e.g. a software, initially, the contents of the respective 128 bit memory word register 609 and the contents of the associated CRC register 61i is read out, as mentioned above. Thereafter, the 9 bit CRC word is regenerated therefrom by CRC arithmetic unit 73 and compared with the read-out CRC word. If these two CRC words do not correspond, an error signal F (or a corresponding error flag) is produced. If the CRC words correspond, a new 9 bit CRC word is calculated from the 128 bit memory word which contains the new 32 bit data word, as has been explained hereinabove, and both are read in the corresponding 128 bit memory word register 60i or the associated 9 bit CRC register 61i of the RAM module, respectively.

The error check can be performed even if it is desired to read out a data word from the RAM module on the data bus 20. For this purpose, the contents of the memory word register 60i that contains the respective data word is transferred into the CRC arithmetic register 72, and the CRC word is recalculated therefrom. This CRC word is compared to the CRC word memorized in the associated CRC word register 61i. If the two words do not correspond, an error message F is generated or a corresponding error flag set. If both CRC words correspond, the read-out 32 bit data word is transferred to the data bus 20.

Thereafter, the contents of the CRC arithmetic register 72 is returned into the corresponding 128 bit memory word register 60i.

Figure 6 shows several memory word registers 10a, 10b,..10x, for 32 bit data words and a 32 bit parity word register 12, wherein a bit with the value 0 or 1 is illustrated for each digit as an example.

In contrast to the word-oriented check bit generation shown in Figures 4 and 5, a column-oriented parity is generated according to Figure 6, wherein for respectively equal digits of all data words a parity bit is determined which is written into an associated digit in the 32 bit parity word register 32. A 32 bit parity word is thus achieved. Further, a 2 bit parity word can be generated and stored in the 2 bit parity word regiser 13 (see Figure 1) with respect to the above 32 bit parity word in the same manner as was described for the word-oriented parity by way of Figure 4. Corresponding to the fashion described hereinabove, a column-oriented parity check can be performed in the embodiment of Figure 5 with 128 bit long data words.

When writing a new data word in one of the word registers 10i of the RAM module, first the contents of the data word of the memory digit being described in the RAM module, i.e., a 32 bit data word register 10i in the present example, and the 32 bit parity word register 12 is read out. Thereafter, the value of the column-oriented 32 bit parity word is determined and described again.

Subsequently, the new data word is re-written in the corresponding data word registers 10i, and the contents of the 32 bit parity word register 12 is re-determined. Following this operation, again a 2 bit parity can be generated with respect

to the 32 bit parity word and stored in the 2 bit parity word register 13 (see Figure 1).

It is preferred that an error check is not performed during a normal reading operation. An additional error check may be carried out in that in the manner described above, e.g. at the point of time during a reading operation, the contents of all data word registers 10i is read out, the column-oriented 32 bit parity word is regenerated and compared with the parity word stored in the parity word register 12. If the parity words do not correspond, an error message F is produced or a corresponding error flag is set. If the parity words correspond, the read-out data word is transferred to the data bus 20. The column-oriented error check in the entire RAM described in the embodiment hereinabove is expediently not performed with each writing or reading operation but at defined intervals, and it is possible that the said intervals are prededetermined by the software used. The decision whether this error check takes place or not is preferably made by the implemented software.

The 2 bit parity word of the 32 bit parity word can be used for error checks in the same way as it was described by way of Figures 2 to 4 for the 2 bit parity words of the data words.

Instead of the column-oriented parity, a column-oriented CRC (Cyclic Redundancy Check) sum may be produced and used for error checks. Before writing and/or reading a word, first the contents of all data word registers 10i and check bit register 12 are read out, and the CRC word is determined again also in this case. If this CRC word does not correspond with the memorized CRC word, an error message F is produced or a corresponding error flag is set. If both CRC words correspond, the writing or reading operation is concluded in the manner

described in the above with respect to the column-oriented parity word generation.

The column-oriented parity and a cyclically occurring parity check or the CRC check sum and a cyclic CRC calculation permit detecting errors in the address decoder as well as double bit errors and further errors. The checks or calculations, respectively, are preferably performed by a corresponding software.

Patent Claims:

1. Method of storing data words in a RAM module,
c h a r a c t e r i z e d by the following method steps:
producing a check bit word from at least one data word when writing the at least one data word into the RAM module,
storing the check bit word,
reading out the check bit word when reading out the at least one data word from the RAM module,
regenerating the check bit word from the at least one read-out data word,
comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond.

2. Method as claimed in claim 1,
c h a r a c t e r i z e d in that the check bit word is generated by determining parity bits.

3. Method as claimed in claim 2,
c h a r a c t e r i z e d in that a 2 bit parity word is generated from each data word, and one parity bit is respectively determined from each data halfword.

4. Method as claimed in claim 1 or 2,
c h a r a c t e r i z e d in that a parity word is generated from a number of data words, and its parity bits are respectively determined from equal digits of all data words.

5. Method as claimed in claim 1,
c h a r a c t e r i z e d in that the check bit words are generated by calculating CRC words.

6. Method as claimed in claim 5,
c h a r a c t e r i z e d in that in each case a number of data words are summed up to form a memory word, and an associated CRC word is calculated therefrom.

7. Circuit configuration for storing data words in a RAM module, c h a r a c t e r i z e d by:
a first circuit unit (21) for generating a check bit word from at least one data word when writing and reading the at least one data word, a number of registers (11i, 61i) for the allocated storage of check bit words for the data words, and a second circuit unit (22) by means of which, when reading data words, the associated check bit word is compared to the check bit word regenerated by the first circuit unit (21), and for generating an error message (F) if the check bit words do not correspond.

8. Circuit configuration as claimed in claim 7,
c h a r a c t e r i z e d in that the number of registers is produced by first 2 bit parity registers (11i), and one 2 bit parity register is associated with each data word.

9. Circuit configuration as claimed in claim 7,
c h a r a c t e r i z e d in that the number of registers is produced by CRC registers (61i), one CRC register being associated in each case with four data words.

10. Circuit configuration as claimed in claim 9,
c h a r a c t e r i z e d by a multiplexer (71) for storing four data words as one memory word, and a CRC arithmetic unit (73) for calculating the CRC word from a memory word and for storing the CRC word in an associated CRC register (61i, 74).

11. Circuit configuration as claimed in claim 10, characterized in that the data words are 32 bit words and the CRC words are 9 bit words.

12. Circuit configuration as claimed in any one of claims 7 to 11,
characterized by a second register (12) for storing a check bit word, the bits of which are respectively determined from equal digits of all data words, and a third register (13) for storing a check bit word which is determined from the contents of the second register (12).

Abstract:

Method and Circuit Configuration for Storing Data Words in a RAM Module

The present invention describes a method of storing data words in a RAM module which is especially suited for applications that are critical in terms of safety and includes the following steps: producing a check bit word from at least one data word when writing the at least one data word into the RAM module, storing the check bit word, reading out the check bit word when reading out the at least one data word from the RAM module, regenerating the check bit word from the at least one read-out data word, comparing the read-out check bit word with the regenerated check bit word and generating an error message if they do not correspond. This invention further relates to a corresponding circuit configuration.

(Figure 3)

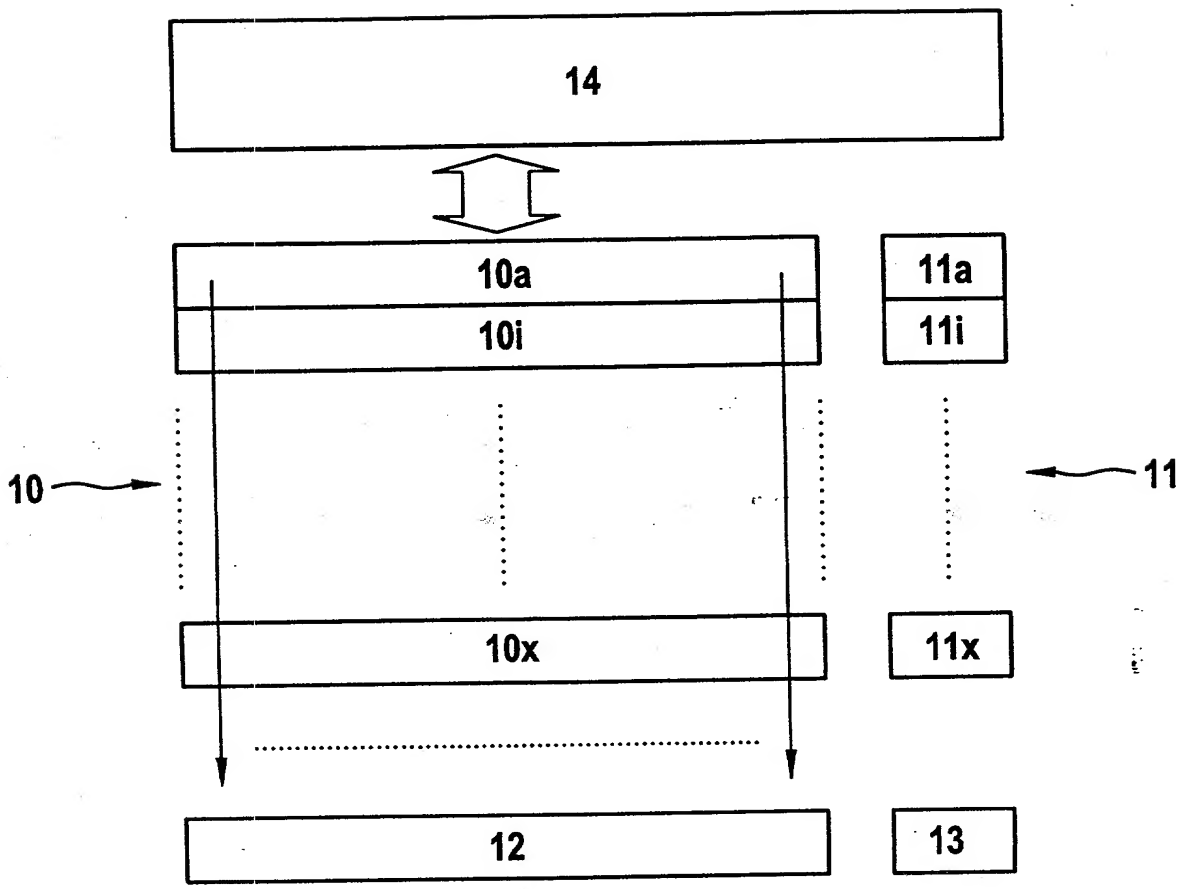

Fig. 1

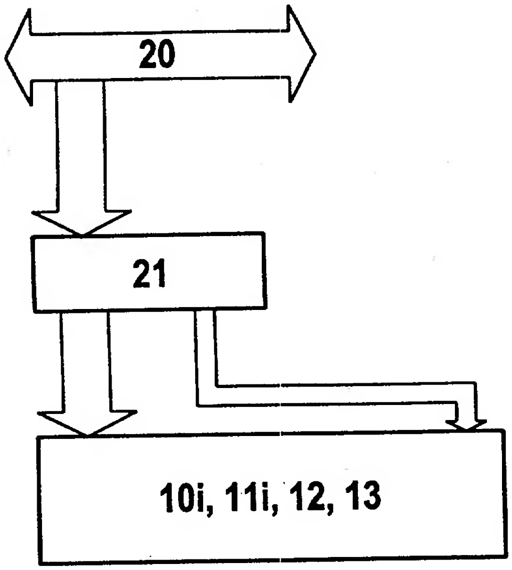

Fig. 2

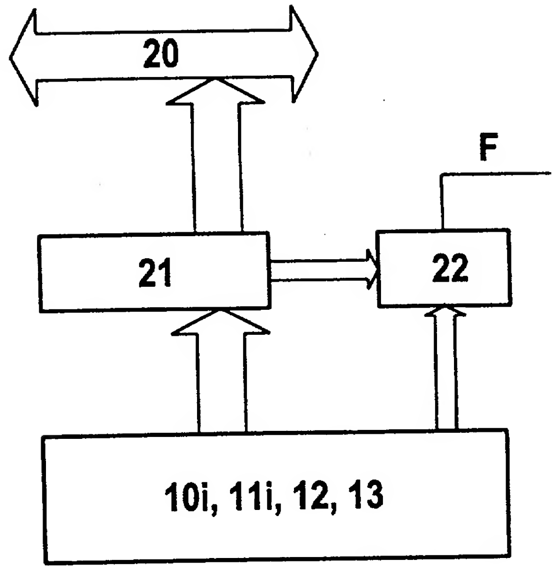

Fig. 3

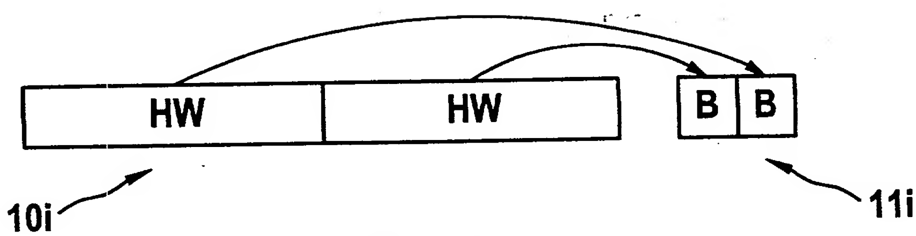

Fig. 4

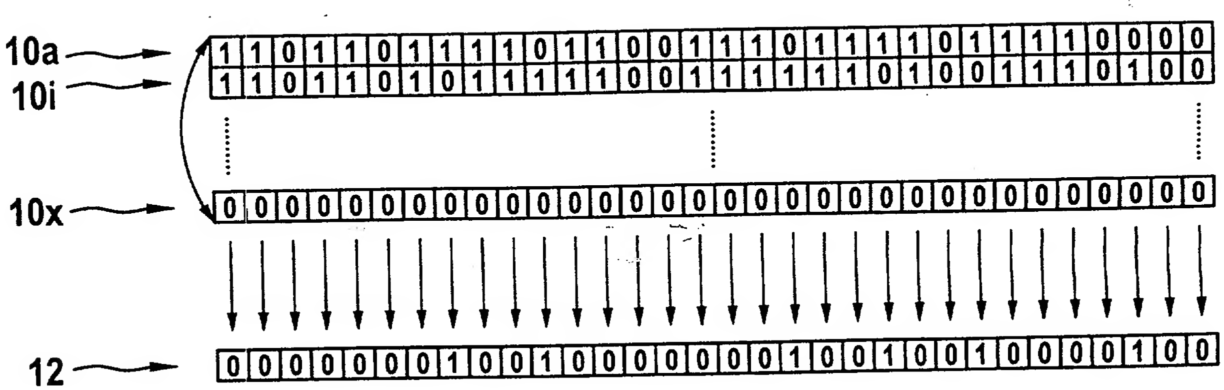

Fig. 6

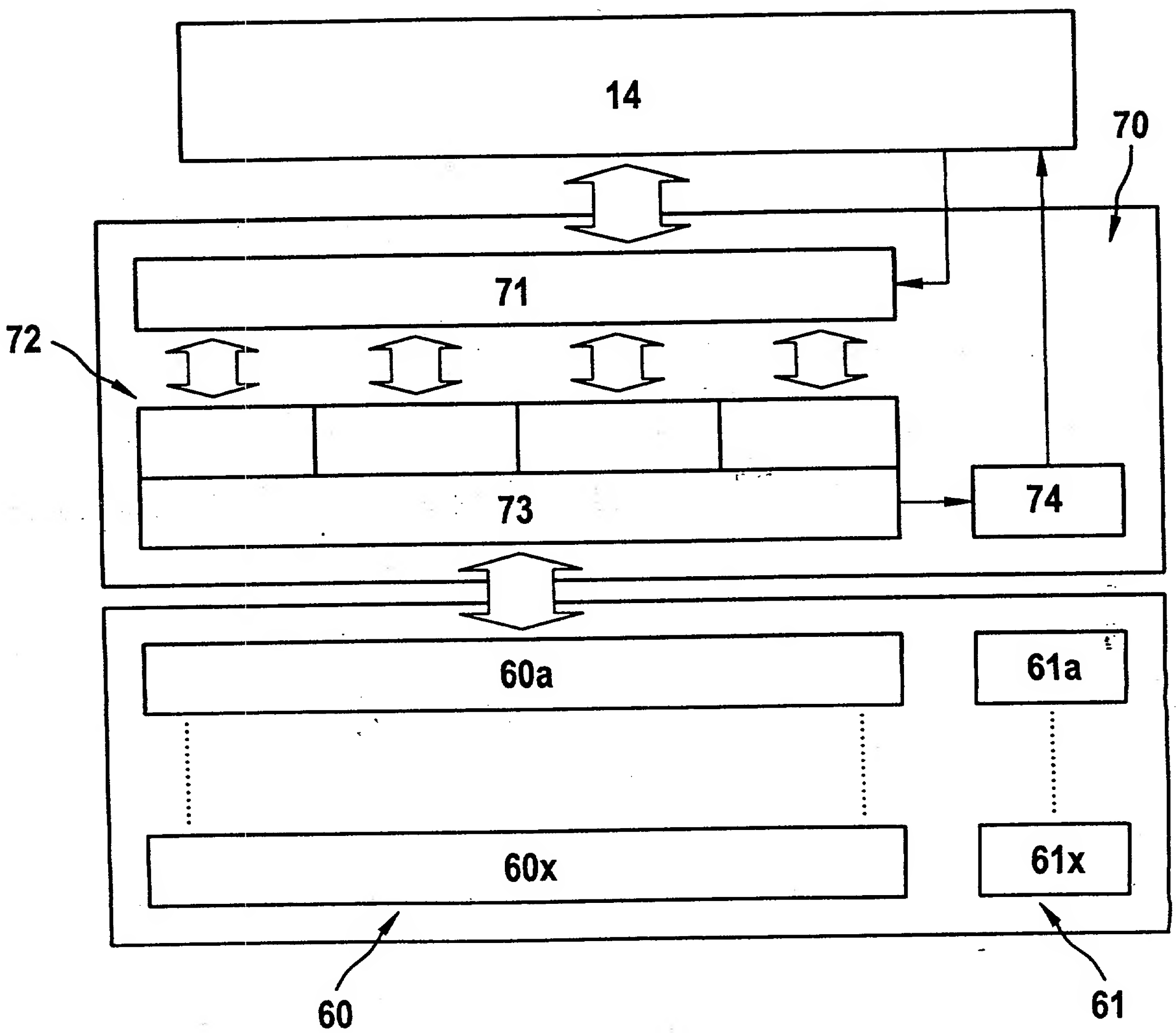

Fig. 5

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Declaration and Power of Attorney for Patent Application
Erklärung für Patentanmeldungen mit Vollmacht

German Language Declaration

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Verfahren und Schaltungsanordnung zum Speichern von Datenworten in einem RAM Modul

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☒ wurde angemeldet am **29.08.2000**
unter der US-Anmeldenummer oder unter der Internationalen Anmeldenummer im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesens (PCT) **PCT/EP 00/08398**

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As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method and Circuit Configuration for Storing Data Words in a RAM Module

the specification of which is attached hereto unless the following box is checked:

☒ was filed on **08/29/2000**
as United States Application Number or PCT International Application Number **PCT/EP 00/08398**

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above and as amended in a preliminary amendment.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

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Prior Foreign Applications (Frühere ausländische Anmeldungen)			Priority Not Claimed Priorität nicht beansprucht
10018722.6	**Germany**	**15/April/2000**	☐
19945494.9	**Germany**	**22/Sept/1999**	
PCT/EP00/08398	**PCT**	**29/Aug/2000**	
Number	Country	Day/Month/Year Filed	☐

Ich beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s)listed below.

Application No. , filed on

Application No. , filed on

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Application No. , filed on

Status: patented/pending/abandoned)

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Status: patented/pending/abandoned)

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Attorney's Docket No: P9722

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